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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,374	01/02/2002	Robert C. Glenn	42390P12279	9816
8791	7590	01/17/2007	EXAMINER	
BLAKELY SOKOLOFF TAYLOR & ZAFMAN			FILE, ERIN M	
12400 WILSHIRE BOULEVARD			ART UNIT	PAPER NUMBER
SEVENTH FLOOR			2611	
LOS ANGELES, CA 90025-1030				
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
3 MONTHS		01/17/2007	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)
	10/039,374	GLENN, ROBERT C.
	Examiner Erin M. File	Art Unit 2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 02 October 2006.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-18 and 20-30 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-3,11,14,25 and 27 is/are rejected.
 7) Claim(s) 4-10,12,13,15,16 and 26 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 11 May 2006 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date: _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date: _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see Remarks, filed 10/2/2006, with respect to the rejection(s) of claim(s) 1-3, 11, 14, 17, 18, 21, 22, 25, 27-30 under Chao in view of Tamura have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Chao and Tamura.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-3, 11, 14, 17, 18, 21, 22, 25, 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chao et al. (U.S. Patent No. 6,380,783) in view of Tamura (U.S. Patent No. 6,826,390).

Claims 1, 17, 25, 28, Chao discloses maintaining a first amplitude of a first interrelated control signal and a second amplitude of a second interrelated control signal (fig. 1, 16, col. 3, lines 43-45, weighted current bias generator maintains IA and IB which are interrelated control signals); amplitude circuitry coupled to increase the first amplitude at a rate substantially equivalent to a rate of decrease in the second amplitude (fig. 6

shows the rate of increase and decrease are the same, further Chao discloses the currents are complementary to each other, col. 2, lines 46-48, col. 4, line 65-col. 5, line 2), to change an amplitude contribution of a reference clock phase, within high and low amplitude boundaries (high and low boundaries are met by constant voltage contribution total, col. 4, lines 28-30) of a substantially small signal region of a transfer characteristic of phase control circuitry of a phase interpolator (see fig. 3, which shows the transfer characteristic of phase control circuitry of the interpolator). Chao fails to disclose the charge storage circuitry for maintaining the control signal amplitudes, however, Tamura discloses sample and hold circuitry in which capacitors are used to store charges used for weighting signals (col. 4, lines 45-65). Because this particular charge storage and weighting system reduces the common node voltage necessary, increasing transmission speed and efficiency (col. 1, lines 50-60), it would have been obvious to one skilled in the art at the time of invention to include the invention as disclosed by Tamura into the invention of Chao.

Claims 2, 18, Chao discloses comprising common mode feedback circuitry coupled with said charge storage circuitry to maintain a substantially consistent common mode voltage between the first amplitude and the second amplitude (weighted current generator 16 includes a constant voltage col. 4, lines 28-30, and complementary first and second currents, col. 2, lines 46-48, creating a consistent common voltage between first amplitude and second amplitude).

Claim 3, wherein the common mode feedback circuitry comprises circuitry to compare the common mode voltage with a reference voltage (transistors 42-48 provide the

reference voltage from the constant power source); and an output coupled to charge circuitry to increase the first amplitude and the second amplitude in response to the common mode voltage being less than the reference voltage, and coupled to discharge circuitry to decrease the first amplitude and the second amplitude in response to the common mode voltage being greater than the reference voltage (col. 5, lines 34-43).

Claim 11, Chao discloses charge storage circuitry to provide a differential interrelated control signal for the reference clock phase (col. 4, line 65-col. 5, line 5). Tamura discloses the use of a capacitor for charge storage circuitry (col. 4, lines 58-59).

Claim 14, Chao discloses amplitude circuitry comprises: charging circuitry to increase the first amplitude; and discharging circuitry to decrease the second amplitude in proportion to an increase in the first amplitude. (col. 4, line 65-col. 5, line 5, Chao discloses that the first and second currents are complementary to each other, $IA + IB = 1$, so that as one charges or increases, the other decreases proportionately).

Claim 21, 29, Chao discloses increasing an amplitude comprises charging a first charge storage circuit to increase the amplitude contribution of the first reference clock phase (col. 4, line 65-col. 5, line 5).

Claim 22, 30, Chao discloses decreasing an amplitude comprises discharging a second charge storage circuit to decrease the amplitude contribution of the second reference clock phase (col. 4, line 65-col. 5, line 5).

Claim 27, Chao discloses charging circuitry to increase the first amplitude; and discharging circuitry to decrease the second amplitude in substantially inverse proportion to an increase in the first amplitude (col. 4, line 65-col. 5, line 5).

Allowable Subject Matter

4. Claims 17-24, 28-30 allowed.
5. Claims 4-10, 12, 13, 15, 16, and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erin M. File whose telephone number is (571)272-6040. The examiner can normally be reached on M-F 1:00PM-9:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Erin M. File

E.M.F.

1/4/2007


MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER